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MS APPEAL BRIEF - PATENTS
Docket No.: 0941-0809P
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Sheng-Chih LAI et al.

Application No.: 10/642,244 | Confirmation No.: 8162

Filed: August 18, 2003 | Art Unit: 2823

For: MASK READ ONLY MEMORY CONTAINING DIODES AND METHOD OF MANUFACTURING THE SAME | Examiner: W. D. Coleman

APPEAL BRIEF TRANSMITTAL FORM

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 23, 2006

Sir:

Transmitted herewith is an Appeal Brief on behalf of the Appellants in connection with the above-identified application.

☐ The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.

A Notice of Appeal was filed on November 23, 2005.

☐ Applicant claims small entity status in accordance with 37 C.F.R. § 1.27.

The fee has been calculated as shown below:

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Dated: January 23, 2006

Respectfully submitted,

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Attachment(s)

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APPEAL BRIEF

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January 23, 2006

Sir:

As required under § 41.37(a), this brief is filed no more than two months after the Notice of Appeal filed in this case on November 23, 2005, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Macronix International Co., Ltd. of Hsin-Chu, Taiwan as recorded in an Assignment found at Reel 014410, Frame 0233 recorded on August 18, 2003.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 20 claims pending in application.

B. Current Status of Claims

1. Claims canceled: None

2. Claims withdrawn from consideration but not canceled: 12-19

3. Claims pending: 1-11 and 20

4. Claims allowed: None

5. Claims rejected: 1-11 and 20

C. Claims On Appeal

The claims on appeal are claims 1-11 and 20

IV. STATUS OF AMENDMENTS

Applicant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the present invention relates to a semiconductor mask read only memory containing diodes. The first embodiment is shown in Fig. 1L and in Fig. 2. The second embodiment is shown in Fig. 3P and Fig. 4. Referring especially to Fig. 1L, a substrate layer 110 has formed thereon an insulating layer 112 and a conductive layer BL (bit line). An N-type semiconductor layer 122 and an P type semiconductor layer are formed thereon to form the diodes. The BL 122 and 124 layers are etched so as to form "pillars" defining separate diodes. An insulator layer 150 covers the top of some of the diodes, but not all of the diodes. A conductive layer WL (word line) is formed on top of the diodes and the insulator layers 150. It should be noted that the WL layer is formed in strips in the B direction while the BL layer is formed in strips in the A direction. The memory distinguishes binary bits "0" and "1" according to whether the insulator layer 150 is present on top of the diode. As shown in Fig. 2, the memory shown in Fig. 1L can be stacked vertically in two or more layers. The second embodiment

shown in Figs. 3P and 4 show a somewhat similar arrangement where the vertically adjacent diodes reverse the order of the N and P layers.

In regard to claim 1, and using the reference numerals found in Fig. 1L, the memory 10 is shown as having a semiconductor substrate 110, an insulating layer 112 on the substrate, a plurality of first conductive lines along first direction BL, a plurality of vertical diodes D (each containing part of layers 122 and 124), a plurality of dielectric layers on the diodes 150 and a plurality of second conductive lines along a second direction WL. Corresponding parts are also found in the second embodiment.

Claim 20, the only other independent claim at issue, likewise shows a memory 10, substrate 110, insulating layer 112, first conductive lines BL and first and second vertical diodes D, where the first diodes are those which have dielectric layer 150 on top and the second diodes are those without the dielectric layer on top. The plurality of dielectric layers are the parts of layer 150 and the plurality of second conductive lines is WL. It should also be noted in regard to both claims 1 and 20 that the dielectric layer 150 is actually formed in strips in the same direction as the word line thus providing "a plurality of dielectric layers."

Claims 4, 6, and 9 describe the materials from which the insulating layer may be made. This list is found in a number of locations in the specification such as page 8, line 28 to page 9, line 2.

Claims 7 and 10 relate to the arrangement shown in Figs. 2 and 4 where there are multiple layers of diodes. Claim 7 describes at least two memory cell layers while claim 10 describes n diode layers.

Claims 8 and 11 describe the number of layers as 2 to 10 (page 3, line 15).

The remaining claims 2, 3 and 5 describe the diodes as PN diodes (page 9, line 10), describe the diodes as two polysilicon layers of opposing types (page 9, lines 13-17) and describe the two conductive lines as bit lines and word lines (page 10, line 12; page 11, lines 17-18).

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

The Examiner has rejected claims 1-11 and 20 under 35 USC 102(e) as being anticipated by Johnson, U.S. Patent 6,525,953. The first question is whether the Johnson reference shows every feature of the claimed invention.

The Examiner has also rejected claims 1-11 and 20 under 35 USC 102(b) as anticipated by Japanese patent publication Abstract 06-334139. The second question is whether the Examiner has met his burden of properly describing how the claims are anticipated by this reference. The third question is whether the reference shows each and every feature of the claimed invention.

VII. ARGUMENT

Rejection Over Johnson

First, it is noted that the Examiner has stated that the rejection refers to claims 1-11 (page 2, paragraph 5 of the Final Rejection). However, the Examiner has also commented on claim 20 in regard to this rejection on page 7, paragraph 18. Accordingly, it is assumed that the Examiner meant to include claim 20 in this rejection.

In answer to Appellant's previous arguments, the Examiner has referred to Col. 1, lines 24-26 and lines 47-60 of the Johnson reference (page 2, paragraph 3 of the Final Rejection). Appellants note that lines 24-26 are part of the background description of the Johnson reference and refer to an earlier patent 6,034,882. Likewise, lines 47-60 relate to an earlier patent application 09/560,626. Since these sections of the Johnson reference do not refer to the Johnson device, but rather to prior art devices, it is not clear how the Examiner can use this teaching to show a dielectric layer formed directly on a diode. Further, it is not clear whether the Examiner is including either of these references as part of the rejection. If so, Appellants submit that this should be an obviousness rejection rather than an anticipation rejection.

The Examiner has pointed out that the Johnson reference shows a semiconductor substrate 100, an insulating layer 102, conductive lines 114 and vertical diodes 12. It is noted that Col. 3, lines 10-15, describe the pillars 12 as having first and second diode components 13 and 14 separated by an anti-fuse layer 16. This is seen best in Fig. 1. Thus, Johnson teaches the use of a disrupted dielectric layer to separate the first and second diode components.

The Examiner then continues to state that the plurality of dielectric layers on the diodes relate to layer 120. However, layer 120 as seen in Fig. 4 is the anti-fuse layer which is part of the vertical diode. This layer does not correspond to the dielectric layer as described in claims 1 and 20 since the claimed layer is "on the diodes." It should also be noted the Examiner has referred to the language present before the last amendment "on part of the diodes." This is incorrect since the Amendment of May 12, 2005.

Thus, Appellants submit that the Examiner has not shown a plurality of dielectric layers on the diodes as required in claim 1. Likewise, the Examiner has not shown the corresponding language in claim 20 that the dielectric layers are "directly on the first vertical diodes." Instead, the Johnson reference only shows the dielectric layer as an anti-fuse layer between the N and P conductive layers. Accordingly, Appellants submit that both claims 1 and 20 are not anticipated by this reference.

Furthermore, in regard to the Examiner's statements in answer to the previous arguments, the section at Col. 1, lines 24-26 refers to an insulator which is placed between the pillars and not "on" the pillars. Thus, this would equate to the insulator 140 shown in Fig. 1L of the present application. Thus, this also does not aid the Johnson reference is describing the claimed invention. In regard to claim 1, lines 47-60, the dielectric fill described in line 52 is again placed between the rail stack materials which is thus similar to the description at Col. 1, lines 24-26 and similar to dielectric 140 of the present invention. Again, this section does not aid the Johnson reference in teaching the claimed invention.

Likewise, the section of the Johnson reference at Col. 13, line 42 and following again relate to the forming of an insulator between the pillars and not "on" the pillars. Thus,

Appellants submit that the Johnson reference does not show this feature in any form. Accordingly, independent claims 1 and 20 are not anticipated by this reference.

In regard to claims 4, 6 and 9, it is noted that while the Examiner states that Johnson shows the insulating layer as being a list of materials, the Examiner has not pointed out anywhere where this list is found in Johnson. Thus, Appellants submit the Examiner has not met his burden of teaching the claimed invention. Further, as noted above, since the insulating layer must be formed on the diodes, Johnson does not show such a layer at all anyway. Appellants do note that the anti-fuse layer 120 is described as being silicon dioxide at Col. 8, line 64. However, as noted above, this layer is not on the diodes. Accordingly, claims 4, 6 and 9 are also not anticipated by this reference.

In regard to claims 8 and 11, the Examiner merely states that the reference shows that the number of layers is 2 to 10. Appellants submit that the Examiner has not met his burden of showing where this is found in the reference. Accordingly, Appellants submit that these claims are also not anticipated by the reference.

Claims 2-11 depend from claim 1 and are also considered to be allowable based on their dependence from allowable claim 1.

Rejection Under JP 06-334139

First, Appellants submit that the Examiner has not met his burden of stating a proper anticipation rejection since there has been no indication of how the reference is being used to reject the claims. Further, since the publication is in the Japanese language, this is especially important since only the English language abstract and drawings can be understood. If the Examiner is relying on anything other than the Abstract and drawings, he is requested to provide a translation of the parts relied on.

+ Likewise, Appellants submit that there is no description of the material described in claims 4, 6 and 9. Further, there is no description of multiple cell layers as described in claims 7, 8, 10 and 11. Accordingly, Appellants that these claims likewise are not anticipated by this reference.

Dependent claims 2-11 are also allowable based on their dependency from allowable claim 1.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: January 23, 2006

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/642,244

1. A mask read only memory containing diodes, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate;

a plurality of first conductive lines along a first direction on the insulating layer;

a plurality of vertical diodes on the first conductive lines;

a plurality of dielectric layers on the diodes; and

a plurality of second conductive lines along a second direction on the dielectric layers and the diodes, wherein the first direction is perpendicular to the second direction.

2. The mask read only memory containing diodes as claimed in claim 1, wherein the diodes are PN diodes.

3. The mask read only memory containing diodes as claimed in claim 2, wherein the PN diodes comprise two polysilicon layers of opposing conductive types.

4. The mask read only memory containing diodes as claimed in claim 1, wherein the insulating layer is silicon dioxide, aluminum oxide (Al2O3), silicon nitride (Si3N4), tantalum pentoxide (Ta2O5), barium strontium titanate (BST), hafnium oxide (HfO2), or titanium dioxide (TiO2).

5. The mask read only memory containing diodes as claimed in claim 1, wherein the first conductive lines are bit lines and the second conductive lines are word lines.

6. The mask read only memory containing diodes as claimed in claim 1, wherein the dielectric layers are silicon dioxide, aluminum oxide (Al2O3), silicon nitride (Si3N4), tantalum pentoxide (Ta2O5), barium strontium titanate (BST), hafnium oxide (HfO2), or titanium dioxide (TiO2).

7. The mask read only memory containing diodes as claimed in claim 1, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate; and

at least two memory cell layers stacked on the insulating layer wherein there is a separating layer between any two memory cell layers to provide insulation and wherein each memory cell layer comprises:

a plurality of first conductive lines along a first direction on the insulating layer;

a plurality of vertical diodes on the first conductive lines;

a plurality of dielectric layers on part of the diodes; and

a plurality of second conductive lines along a second direction on the dielectric layers and the diodes, wherein the first direction is perpendicular to the second direction,

wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides thereof of opposing conductive type face each other.

8. The mask read only memory containing diodes as claimed in claim 7, which comprises 2 to 10 memory cell layers.

9. The mask read only memory containing diodes as claimed in claim 7, wherein the separating layer is silicon dioxide, aluminum oxide (Al2O3), silicon nitride (Si3N4), tantalum

pentoxide (Ta2O5), barium strontium titanate (BST), hafnium oxide (HfO2), or titanium dioxide (TiO2).

10. The mask read only memory containing diodes as claimed in claim 1, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate;

n diode layers stacked on the insulating layer, wherein n is an integer equal to or greater than 2 and each diode layer comprises a plurality of vertical diodes and a plurality of dielectric layers on part of the diodes; and

(n + 1) parallel conductive layers disposed between the bottom diode layer and the insulating layer, on the top diode layer, and between any two adjacent diode layers respectively, wherein the (n + 1) parallel conductive layers are disposed so that any two adjacent conductive layers are perpendicular to each other,

wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides of matching conductive type face each other.

11. The mask read only memory containing diodes as claimed in claim 10, wherein n is between 2 and 10.

20. A mask read only memory containing diodes, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate;

a plurality of first conductive lines along a first direction on the insulating layer;

first and second vertical diodes on the first conductive lines;

a plurality of dielectric layers directly on the first vertical diodes; and

a plurality of second conductive lines along a second direction directly on the dielectric layers and the second vertical diodes, wherein the first direction is perpendicular to the second direction.